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HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. In other documentation, to reduce potential confusion, the only change to product numbers and names has been in the company name prefix: where a product number/name was HP XXXX the current name/number is now Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

User's Guide

Publication Number E2468-97000
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For Safety Information, Warranties, and Regulatory Information, see the pages at the end of this manual.

HP E2468A PowerPC 403GA Preprocessor Interface

The HP E2468A Preprocessor Interface—At a Glance

The HP E2468A Preprocessor Interface provides a complete interface for state or timing analysis between any PowerPC 403GA target system and the following HP logic analyzers:

- HP 16550A (one or two card)
- HP 16554A (two or three card)
- HP 16555A (two or three card)
- HP 16556A (two or three card)
- HP 1660A/61A

These logic analyzers support various combinations of mixed state/timing analysis. The 403GA configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with the 403GA microprocessors. The inverse assembler allows you to obtain displays of 403GA data in 403GA assembly language mnemonics.

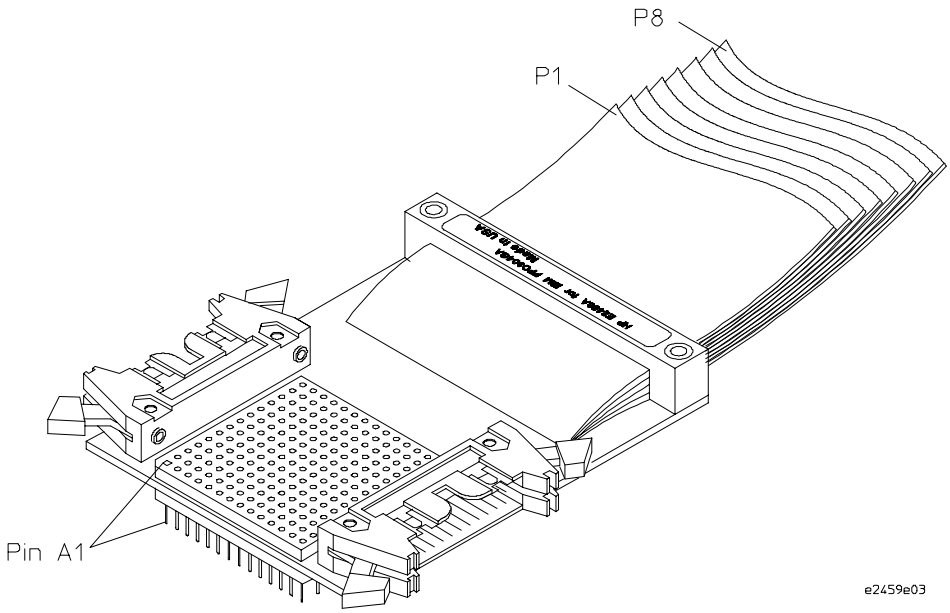

Figure 1. HP E2468A Preprocessor Interface Assembly

In This Book

This book is the user's guide for the HP E2468A Preprocessor Interface. It assumes that you have a working knowledge of the logic analyzer used and the microprocessor being analyzed.

This user's guide is organized into three chapters:

Chapter 1 explains how to attach the preprocessor to the target and how to configure the logic analyzer for state and/or timing analysis.

Chapter 2 provides reference information on the format specification and symbols configured by the preprocessor interface software and information about the inverse assembler and status encoding.

Chapter 3 contains reference information on the preprocessor interface hardware, including the characteristics and signal mapping for the preprocessor interface.

For more information on the logic analyzers or microprocessor, refer to the appropriate reference manual for those products.

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Setting Up the Preprocessor Interface

Setting Up the Preprocessor Interface

This chapter explains how to set up the HP E2468A Preprocessor Interface hardware and software, configure the preprocessor, and connect the preprocessor to supported logic analyzers.

Before You Begin

This section lists the logic analyzers supported by the HP E2468A and provides other information about the analyzers and the preprocessor interface. Before you use the HP E2468A software, use the Duplicate Disk operation in the disk menu of your logic analyzer to make a duplicate copy of the HP E2468A master disk. Then store the master disk and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the disk wears out, is damaged, or a file is accidentally deleted.

Equipment Supplied

The HP E2468A preprocessor interface consists of the following equipment:

- The preprocessor interface hardware, which includes the preprocessor circuit card and cables.
- The configuration files and inverse assembler software on two 3.5-inch disks.
- This User's Guide.

Note: **The preprocessor interface socket assembly pins are covered for shipment with either a conductive foam wafer or a conductive plastic pin protector. This is done to protect the delicate gold plated pins of the assembly from damage due to impact. When you're not using the preprocessor interface, protect the socket assembly pins from damage by covering them with the foam or plastic pin protector.**

Minimum Equipment Required

- The HP E2468A preprocessor interface.
- An HP E5335A Probe Adapter.
- The configuration and inverse assembler software on a 3.5-inch disk.
- One of the logic analyzers listed in the following table:

Table 1. Logic Analyzers Supported

Logic Analyzer	Channel Count	State Speed	Timing Speed	Memory Depth
16550A(one or two card	102	100 MHz	250 MHz	4 k states
16554A (two or three card)	68	70 MHz	125 MHz	500 k states
16555A (two or three card)	68	110 MHz	250 MHz	1 M states
16556A (two or three card)	68	100 MHz	200 MHz	1 M states
1660A/1661A	136/102	100 MHz	250 MHz	4 k states

Setting Up the Preprocessor Interface Hardware

Setting up the preprocessor interface hardware consists of the following major steps:

- Turn off the logic analyzer and the target system.

Caution

To protect your equipment, remove the power from both the logic analyzer and the target system before you make or break connections. Because the logic analyzer supplies power to the preprocessor interface, the logic analyzer should always be powered up before the target system; when powering down, power down the target system first and then power down the logic analyzer.

- Attach the 160-pin PQFP probe adapter (HP E5335A) to the target system.
- Connect the preprocessor interface to the probe adapter.
- Connect the logic analyzer pods to the cable connectors of the preprocessor interface board as shown in Tables 2 through 6.
- Load the logic analyzer configuration by loading the appropriate configuration file.

  Please see Table 7 for corresponding files.

  The remainder of this section describes these general steps in more detail.

To power up or power down

When powering up, the logic analyzer should be powered up first, followed by the target system.

When powering down, the target system should be powered down first, followed by the logic analyzer.

To connect the preprocessor to the target system

Figure 2 shows the connection between the preprocessor interface, the probe adapter, and the target system microprocessor.

- To prevent equipment damage, remove power from both the logic analyzer and the target system.
- Using the instructions in the probe adapter manual, connect the probe adapter assembly to the target system microprocessor. Ensure that pin 1 and A1 are properly aligned.

  The preprocessor interface requires a probe adapter for connecting to the 403GA microprocessor. The probe adapter assembly allows the preprocessor interface to be connected without removing the microprocessor from the target system.
- If desired or needed, attach the flex adapter (HP E3426-60001) to relieve any stress on the probe adapter caused by the weight of the preprocessor. Refer to "Using the flex adapter" for instructions on attaching the flex adapter to the probe adapter.
- Install the preprocessor interface into the PGA socket on the PQFP probe adapter assembly. Again, ensure that pin A1 is properly aligned (see figure 2).

Caution

Serious damage to the target system or preprocessor interface can result from incorrect connection. Note the position of pin 1 and pin A1 on the preprocessor interface, probe adapter assembly, and microprocessor prior to making any connection. Also, take care to align the preprocessor interface connector with the pins on the probe adapter assembly so that all pins are making contact.

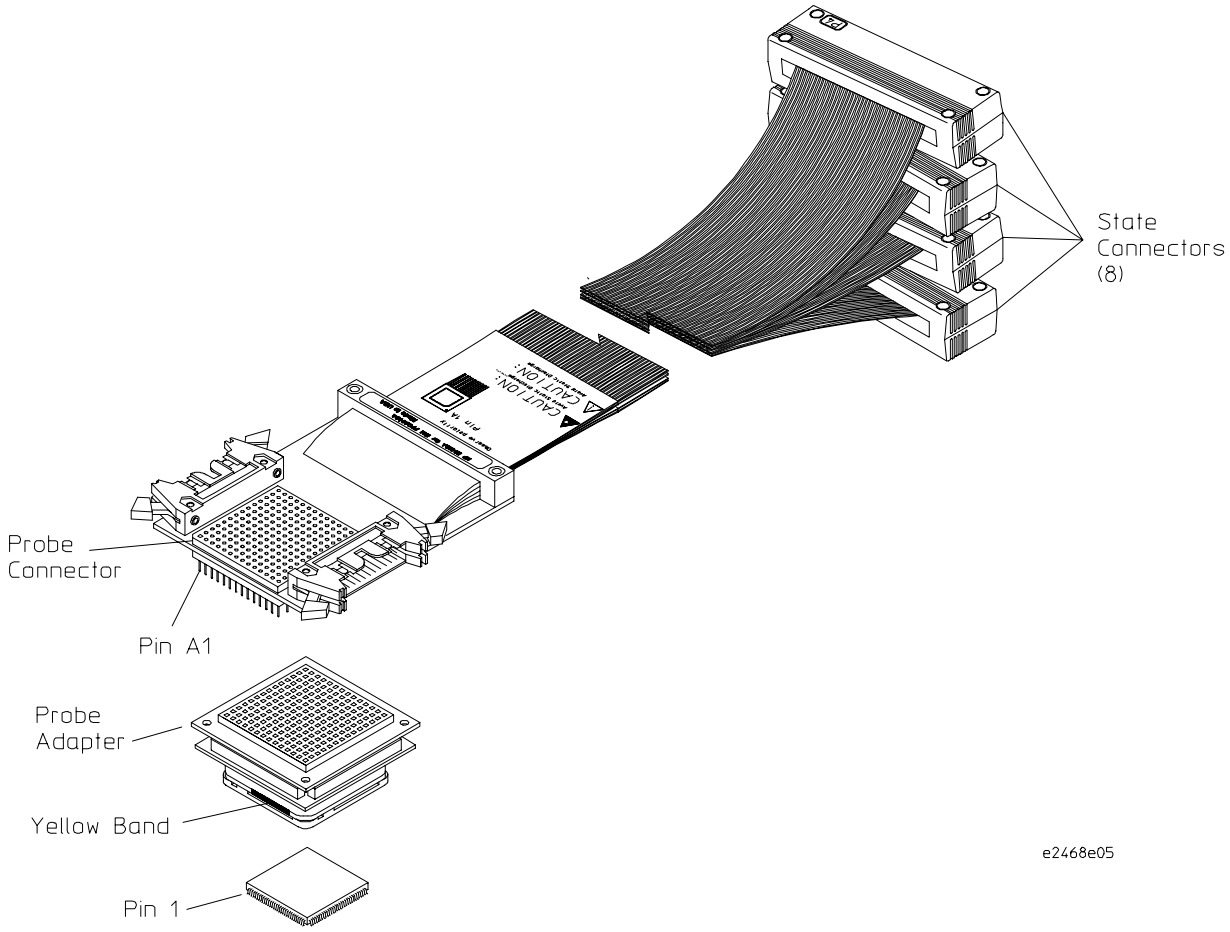

Figure 2. Connecting to the Target System

Using the flex adapter

The HP E3426-60001 flex adapter is designed to relieve mechanical stress and to provide a degree of freedom between the probe adapter and the preprocessor. It is rotation independent. Figure 3 shows the location of the flex adapter, if it is used.

To connect the flex adapter:

- Choose a rotation of the flex adapter that provides the desired flexibility for the preprocessor. The rotation of the flex adapter does not affect electrical connectivity. Note, however, that the preprocessor pin A1 must still be aligned with the microprocessor pin 1.
- Attach the flex adapter to the probe adapter.
- Fold the open end of the flex adapter onto itself. Position and attach the preprocessor to the flex adapter, aligning preprocessor pin A1 directly above the microprocessor pin 1.

Note:

The flex adapter contains a 15 x 15 array of pins, while the preprocessor contains only 14 x 14. When the flex adapter is folded over, there is a 1:1 correspondence between vertical pins. Be sure to attach the preprocessor to the same set of pins attached to the target system.

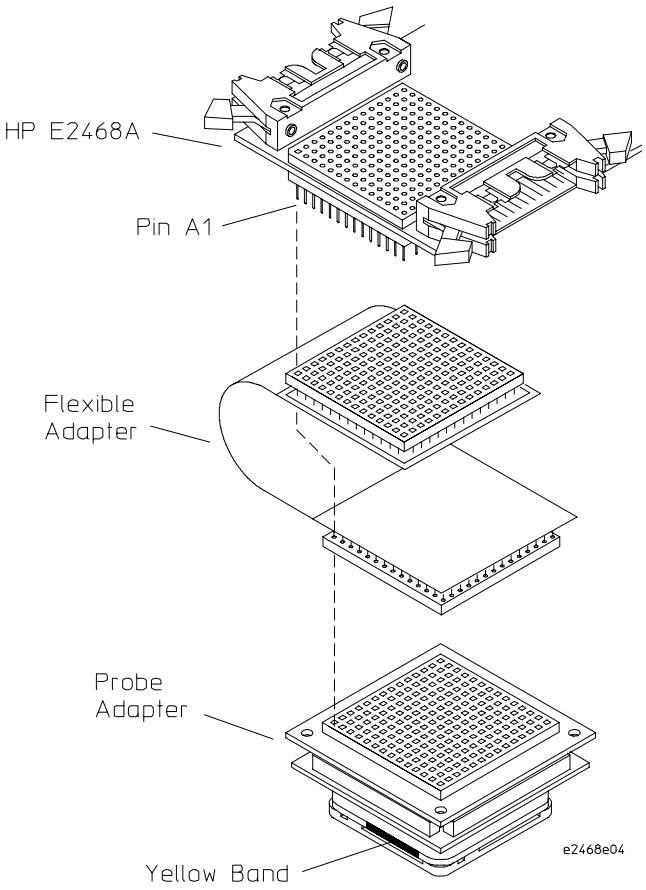

Figure 3. Using the Flex Adapter

Use the figures and tables in the following sections to connect the logic analyzer probes to the cable connectors of the preprocessor interface. Designations such as P1 refer to connectors on the preprocessor interface, while Pod 1 refers to a logic analyzer pod.

To connect to the HP 16554A/55A/56A logic analyzer

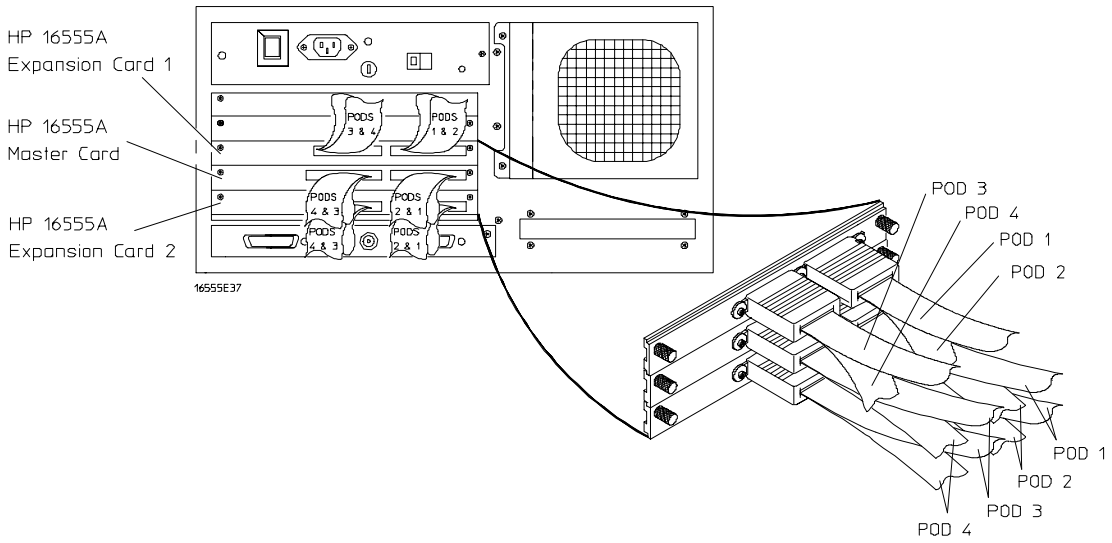

Figure 4. HP 16554A/55A/56A Logic Analyzer Pods

Table 2. Two-card HP 16554A/55A/56A Logic Analyzer Connections

	Pod 4	**Pod 3**	**Pod 2**	**Pod 1**
Expansion Card 1	P1 ADDR	P2 ADDR	P3 DATA	P4 DATA
Master Card	P5 STAT clk↑	P6 DMA	P7 DRAM	P8 JTAG

Use configuration file **C403M** or **CU403M**

Table 3. Three-card HP 16554A/55A/56A Logic Analyzer Connections

	Pod 4	**Pod 3**	**Pod 2**	**Pod 1**
Expansion Card 1	P1 ADDR	P2 ADDR	P3 DATA	P4 DATA
Master Card	P5 STAT clk↑	P6 DMA		
Expansion Card 2			P7 DRAM	P8 JTAG

Use configuration file **C403M3** or **CU403M3**

To connect to the HP 1660A/AS logic analyzer

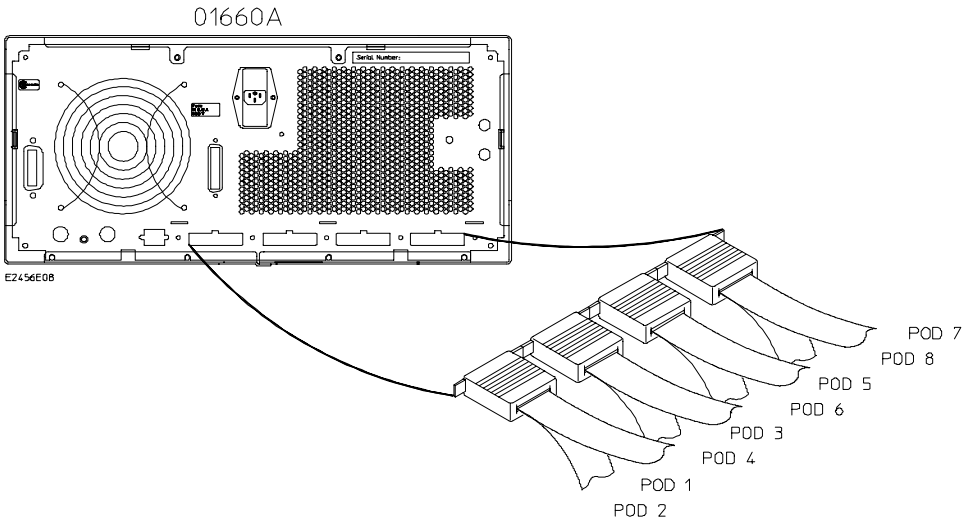

Figure 5. HP 1660A/AS Logic Analyzer Pods

Table 4. HP 1660A/AS Connections

	Pod 8	**Pod 7**	**Pod 6**	**Pod 5**	**Pod 4**	**Pod 3**	**Pod 2**	**Pod 1**
HP 1660A	P1 ADDR	P2 ADDR	P6 DMA	P8 JTAG	P3 DATA	P4 DATA	P5 STAT clk↑	P7 DRAM
Use configuration file **C403J** or **CU403J**								

To connect to the HP 16550A and HP 1661A/AS logic analyzers

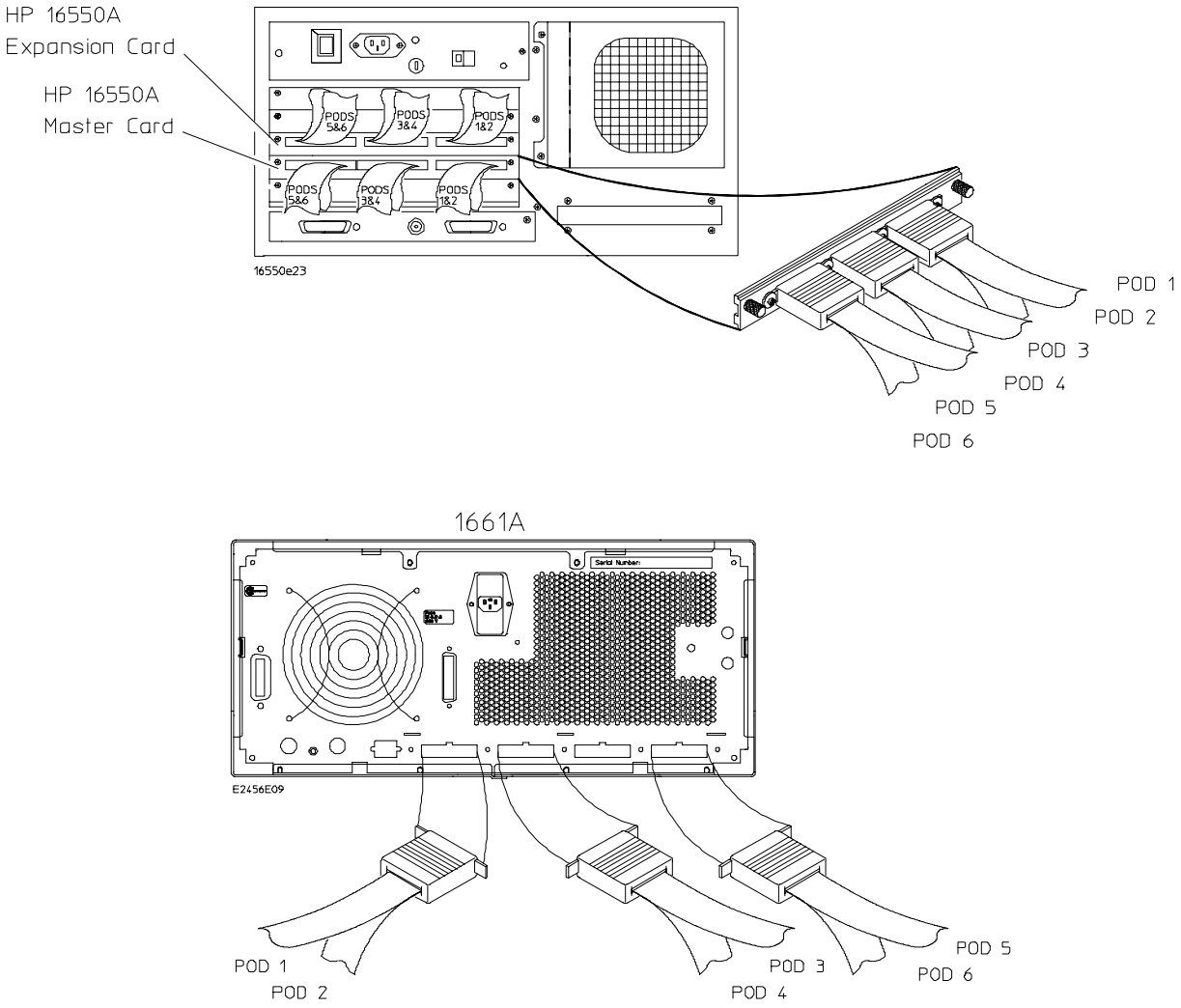

Figure 6. HP 16550A and HP 1661A Logic Analyzer Pods

Table 5. Two-card HP 16550A Logic Analyzer Connections

	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
Expansion Card	P6 DMA	P8 JTAG	P1 ADDR	P2 ADDR	P3 DATA	P4 DATA
Master Card	P5 STAT clk↑	P7 DRAM				

Use configuration file **C403F2** or **CU403F2**

Table 6. One-card HP 16550A Logic Analyzer and HP 1661A/AS Connections

	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 16550A Master Card or HP 1661A	P1 ADDR	P2 ADDR	P3 DATA	P4 DATA	P5 STAT clk↑	*

Use configuration file **C403F** or **CU403F**
*This logic analyzer pod can be connected to P6, P7, or P8, depending on the analysis requirements

Loading the Preprocessor Interface Software

The logic analyzer can be configured for 403GA analysis by loading the appropriate configuration file. Loading this file automatically loads the inverse assembler file. To load the configuration and inverse assembler:

1. **Make a duplicate copy of the master disks prior to setting up the preprocessor interface.**
2. **Insert the appropriate HP E2468A disk into the logic analyzer (see "To select the proper configuration file").**
3. **Depending on your logic analyzer, select one of the following menus:**
   - For the HP 1660-series logic analyzers, select the "System Disk" menu.
   - For the HP 16500A mainframe, select the "System Front Disk" menu.
   - For the HP 16500B mainframe, select the "System Flexible Disk" menu.
4. **Configure the menu to "Load" the analyzer configuration from disk.**
5. **Select the appropriate module (such as "100/500 MHz LA" or "Analyzer") for the load.**
6. **Use the knob to select the appropriate configuration file.**

   Your configuration file choice depends on which analyzer you are using and the type of measurements you want to make. The configuration file names are located at the bottom of the table showing the connections for your particular logic analyzer, and are also located in table 7. The next section describes the differences between the configuration files.
7. **Execute the load operation to load the file into the logic analyzer.**

   The logic analyzer is configured for 403GA analysis by loading the appropriate configuration file. Loading this file also automatically loads the correct inverse assembler.

To select the proper configuration file

There are two configuration files for each analyzer, contained on two disks. One disk contains configuration file is for systems that have IOTV (input/output transaction valid) enabled, and one is for systems that have IOTV disabled. IOTV is used as a storage qualification term; in its absence, the logic analyzer uses state-per-clock capture, and the amount of information captured by the logic analyzer is reduced. Chapter 2 contains information on how to enable IOTV.

Table 7 summarizes the configuration files:

Table 7. Configuration Files

analyzer	403 IOTV	403 st/clk
2-card 16554/55/56	C403M	CU403M
3-card 16554/55/56	C403M3	CU403M3
2-card 16550	C403F2	CU403F2
1-card 16550	C403F	CU403F
1660	C403J	CU403J
1661	C403F	CU403F

To set up the analyzer for timing

The same format specification loaded for state analysis is also used for timing analysis. To configure the logic analyzer for timing analysis:

1. Select the Configuration menu of the logic analyzer.
2. Select the Type field for the analyzer and select Timing.

To Connect to the JTAG Interface

The HP E2468A provides a 2 x 8 connector for interfacing to the JTAG port of the 403GA. The definition of the connector is shown below. Figure 7 shows the pinout.

Table 8. JTAG Interface Signals

Signal	Pin #	Pin #	Signal
JTAG Test Data Out	1	2	reserved
JTAG Test Data In	3	4	reserved
reserved	5	6	Processor Power OK
JTAG Test Clock	7	8	reserved
JTAG Test Mode Select	9	10	reserved
Processor Halt	11	12	reserved
reserved	13	14	no pin
reserved	15	16	ground

JTAG Test Data Out is an output from the 403GA. JTAG Test Data In, JTAG Test Clock, JTAG Test Mode Select, and Processor Halt are inputs to the 403GA. Processor Power OK is an output from the target hardware signaling that the voltage on the target board is at its nominal value.

Processor Halt is a low true signal.

To Connect to the Trace Status Interface

The HP E2468A provides a 2 x 10 connector for monitoring the trace status signals TS0 - TS6. These signals give a real-time identification of the type of cycle being performed. The definition of the connector is shown below. Figure 7 shows the pinout.

Table 9. Trace Status Interface

Signal	Pin #	Pin #	Signal
	1	2	
	3	4	
	5	6	
	7	8	
	9	10	
	11	12	
TS0	13	14	TS1
TS2	15	16	TS3
TS4	17	18	TS5
TS6	19	20	ground

This interface may be connected to the logic analyzer using an HP 01650-63203 termination adapter.

All signals are outputs.

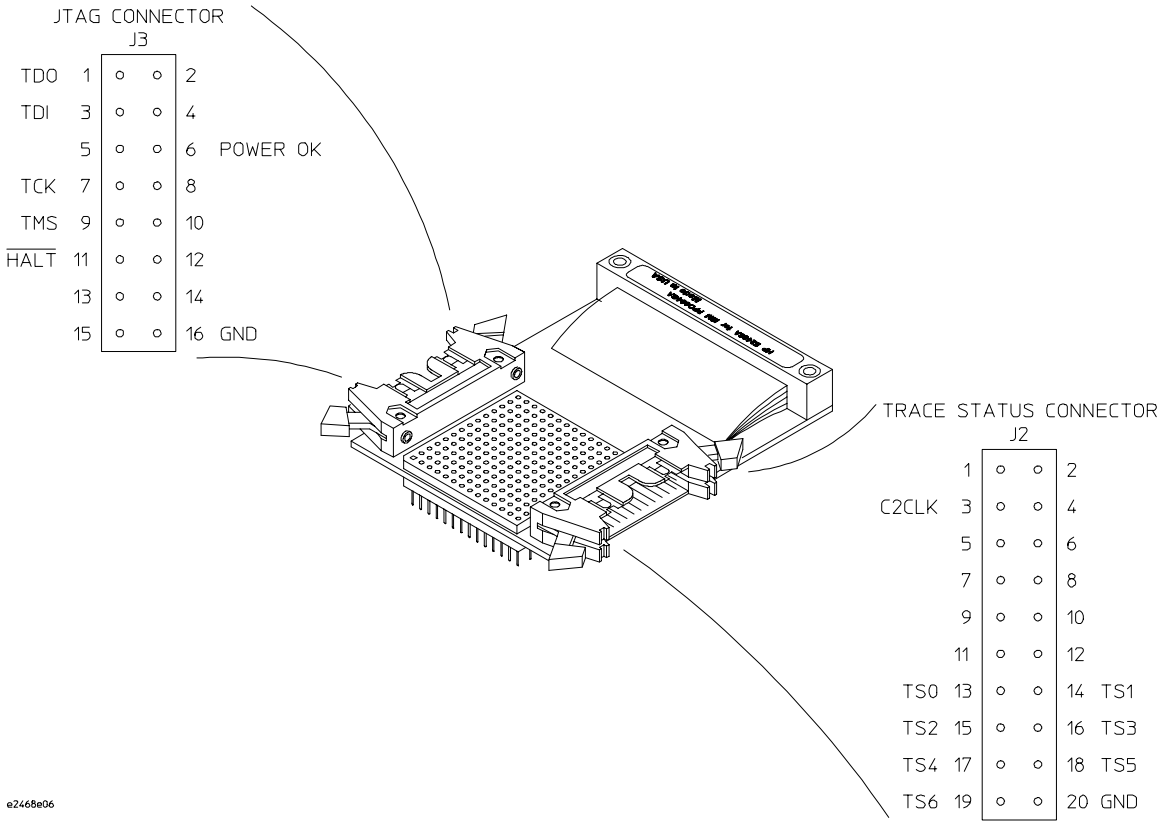

Figure 7. JTAG and Trace Signal Connector Pinouts

2

Analyzing the PowerPC 403GA

Analyzing the PowerPC 403GA

This chapter provides reference information on the format specification and symbols configured by the HP E2468A software. It also provides information about the inverse assembler and status encoding.

Format Specification

When you use the HP E2468A preprocessor interface, the format specification set up by the software will be similar to the following two format specification figures. There may be some slight differences in the displays depending on which logic analyzer you are using and which processor you are probing.

Table 13 in chapter 3 lists the 403GA signals for the HP E2468A preprocessor interface and their corresponding lines to the logic analyzer.

Note

Do not modify the ADDR, DATA, or STAT labels in the format specification if you want inverse assembly. Changes may cause incorrect results. Also note that if the trace specification is modified to store only selected bus cycles, incorrect or incomplete inverse assembly may result. This section describes how to display analyzer configuration information, state and timing data captured by the preprocessor interface, and symbol information that has been set up by the preprocessor interface configuration software.

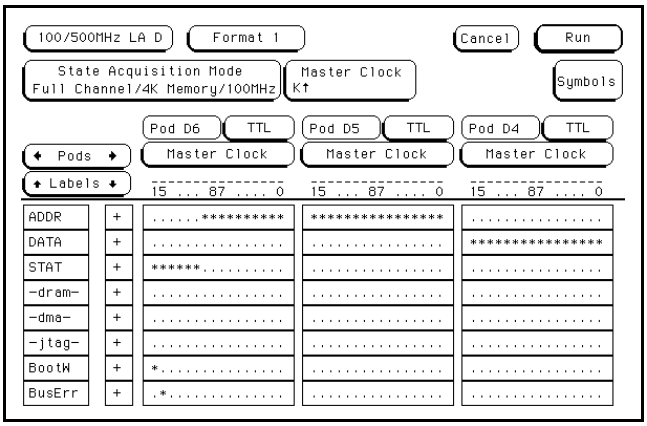

Figure 8. Format Specification (Pods 4-6)

Note

In these format specifications additional labels and pod assignments are listed off the screen. Select the "Labels" field and rotate the knob on the analyzer front panel to view additional signals. Select the "Pods" field and rotate the knob to view other pod-bit assignments. There may be some slight differences in the display shown by your particular analyzer.

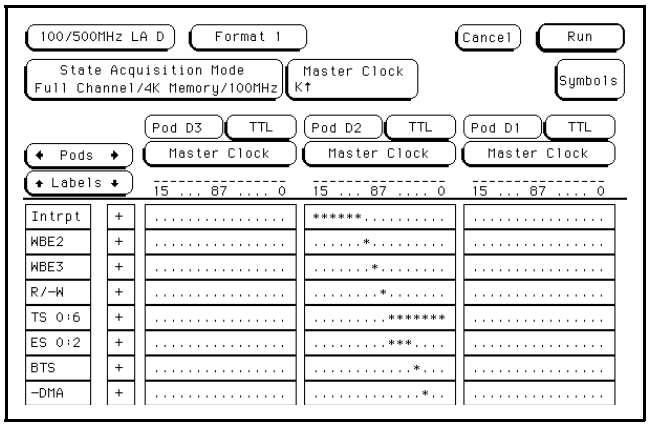

Figure 9. Format Specification (Pods 1-3)

To display the symbols

- Select the "Symbols" field on the format specification menu and then choose a label name from the "Label" pop-up. The logic analyzer will display the symbols associated with the label.

  The HP E2468A configuration software sets up symbol tables on the logic analyzers. The tables contain alphanumeric symbols which identify data patterns or ranges. Labels have been defined in the format specification menu to make triggering on specific 403GA cycles easier. The label base in the symbols menu is set to hexadecimal to conserve space in the listing menu.

  The following tables describe the PowerPC status signals and list the label and symbol encodings defined by the logic analyzer configuration software.

Table 10. STAT Label Bits

Pod P1 STAT Bits (21 - 16)								
STAT Bit			21	20	19	18	17	16
Signal			BootW	BusErr	Error	HoldAck	WBE0	WBE1
Pod P5 STAT Bits (15 - 8)								
STAT Bit	15	14	13	12	11	10	9	8
Signal	INT0	INT1	INT2	INT3	INT4	CINT	WBE2	WBE3
Pod P5 STAT Bits (7 - 0)								
STAT Bit	7	6	5	4	3	2	1	0
Signal	R/W-	ES0	ES1	ES2	BTS	DMA-	I/D-	IOTV

Table 11. Symbol Description

Label	Symbol	403GA Encoding
STAT	pgm	xx xxxx xxxx xxxx 1xxx x111
	rd data	xx xxxx xxxx xxxx 1xxx x101
	wr data	xx xxxx xxxx xxxx 0xxx x111
	data	xx xxxx xxxx xxxx xxxx x111
	IOTV	xx xxxx xxxx xxxx xxxx xxx1
R/-W	rd	1
	wr	0
IOTV	(blank)	0
	valid transfer	1
ERROR	(blank)	0
	error	1
BusErr	bus error	0
	(blank)	1

Trigger Menu

This section describes some PowerPC considerations in triggering the analyzer. The trigger menu determines what will be acquired by the analyzer and when it will be acquired. The HP E2468A software preconfigures a storage qualification term to exclude wait and idle states from the analyzer's memory.

To use the trigger menu

The power-up default on the 403GA has the Real-Time Debug Mode (RDM) bits in the Input/Output Control Register (IOCR) cleared, so that Trace Status outputs (TS 0:6) are disabled. In this condition there are no status signals to indicate when the address and data busses are valid.

A state-per-clock configuration file is provided for this case, along with a state-per-clock inverse assembler, which infers valid states from changes in the address bus and Write Byte Enable signals.

The following code sequence will configure the RDM bits in the IOCR to Bus Status mode (%01):

```
mfdcr   r10,IOCR
rlwinm  r10,r10,0,29,26         # clear bits 27 28
ori     r10,r10,8               # set bit 28
mtdcr   IOCR,r10
```

In this mode, the lower TS bits are assigned the following functions:

TS 0	IOTV	Input Output Transaction Valid
TS 1	I/-D	Instruction 1, Data 0
TS 2	-DMA	Processor Cycle 1, DMA Cycle 0
TS 3	BTS	Bus Transfer Start

An IOTV-aware configuration and disassembler are provided for this case. The trigger specification uses storage qualification to store only states in which IOTV is asserted.

This section discusses the general output format of the inverse assemblers and microprocessor-specific information.

To display captured state data

- **Select the Listing Menu for your logic analyzer.**
  The logic analyzer displays captured data in the Listing Menu. The inverse assembler display is obtained by setting the base for the DATA label to Invasm. Figure 10 shows the Listing Menu as configured on the HP 16550A.

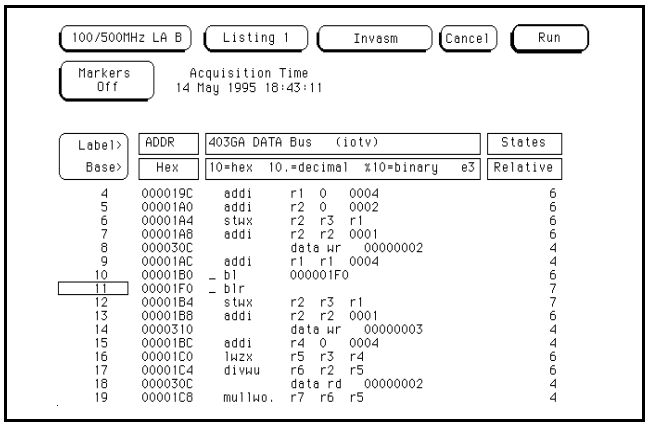

Figure 10. Listing Menu as configured on the HP 16550A

The left-hand column may contain an underscore "_", which indicates a break in the sequential flow of instruction addresses.

The second column displays overfetch and branch-and-link indicators as described in the overfetch marking section on page 2-11. The remaining disassembly listing resembles an assembly listing.

Interpreting Data

General purpose registers are displayed as r0, r1, r2, ..., r31. Condition registers are displayed as cr0, cr1, ..., cr7. Special purpose registers are displayed using their mnemonic.

Most numerical data is displayed in hexadecimal, e.g., "lwz r28 0044(r1)".

Bit numbers and shift counts are displayed in decimal with a dot suffix, e.g., "cror 31. 31. 31.".

A few instructions display their operands in binary with a % prefix, e.g., "mtcrf %00110000 r7".

The disassemblers decode the full PowerPC instruction set architecture, including 64-bit mode instructions and optional instructions not implemented on the 403GA. When these unimplemented opcodes are encountered, the instruction mnemonic has a "?" prefix. If a reserved bit is set in an instruction opcode field, a "?" is appended to the mnemonic, or in some cases to an operand.

An instruction word of 0000 0000 is decoded as "illegal". Otherwise, if an opcode is not valid, it is shown as "Undefined Opcode".

Branch instruction

If a branch hint is encoded, a "+" (for predicted taken) or a minus "-" (for predicted not taken) is appended to the conditional branch mnemonic.

Extended mnemonics

PowerPC assemblers support a number of extended mnemonics for some popular assembly language instructions. The HP E2468A disassembler supports the following dialect:

- Conditional traps and branches decode the condition mnemonically when possible. For some conditions which have no conventional mnemonics (for example, "signed less than or unsigned greater than"), the condition field is displayed in binary.
- The L bit is omitted as a compare operand. Instead, compares are decoded as "cmpw" (or "?cmpd").
- "Add immediate" instructions with a negative immediate operand are decoded as subtract immediate ("subi").
- "Subtract from" instructions "subf" and "subfc" are decoded as subtract instructions sub and subc with the source operands exchanged so that "sub r3 r4 r5" is mnemonically interpreted as "r3 = r4 - r5".
- ori r0 r0 0000 is decoded as "nop".

The following listing shows the extended mnemonics for the integer rotate instructions.

Mnemonic	Decoded As	
rlwimi (rotate left word immediate then mask insert)	inslwi	insert from left immediate
	insrwi	insert from right immediate
rlwinm (rotate left word immediate then AND with mask)	rotlwi	rotate left immediate
	rotrwi	rotate right immediate
	slwi	shift left immediate
	srwi	shift right immediate
	extlwi	extract and left justify immediate
	extrwi	extract and right justify immediate
	clrlwi	clear left immediate
	clrrwi	clear right immediate
	clrlslwi	clear left and shift left immediate
rlwnm (rotate left word then AND with mask)	rotlw	rotate left

Overfetch Marking

Overfetch refers to instructions that are are fetched but not executed by the microprocessor. They may arise from the following sources:

- When bursting, the 403GA first fetches the critical word. The memory system then provides succeeding words. If the critical word was not the first word of the four-word line, the memory system wraps at the line boundary to the first word. Fetches after the line wrap are not in the sequential execution path and are marked with an asterisk "*".
- When the microprocessors execute a branch instruction, the instructions between the branch and the branch target are not executed. These instructions are indicated with a hyphen "-". If the instruction cache is enabled, the branch target may already be in the cache and will not be fetched over the bus. The remaining cache line containing the branch will be marked as overfetch.

An exception to the above includes branches with the link bit set that record the next instruction address in the link register ("lr"). Frequently, these are subroutine branches which will return to the instructions following the branch. These branch-and-link instructions are indicated by a ">".

For conditional branches whose target addresses are not known or are known but not seen in the bus traffic, the inverse assembler cannot always determine if the branch was taken and will not mark ensuing states as overfetch.

Enabling IOTV (PowerPC 403GA)

To enable IOTV, the 403 microprocessor IOCR (configuration register) can be programmed with bits 27..28 set to b'01', i.e., Bus Status Mode. With supervisor access, the following code will accomplish this:

```
mfdcr    r10,iocr        # device control reg x'a0'
andi.    r11,r10,xFFE7   # clear bits 0..15 27 28
ori      r11,r11,8       # set bit 28
andis.   r12,r10,xFFFF   # copy bits 0..15
or       r12,r12,r11     # join bits 16..31
mtdcr    iocr,r12        # device control reg x'a0'
```

With Bus Status Mode disabled, there are no signals on the 403GA to distinguish an opcode fetch from an operand fetch.

To use the Invasm key

The disassembler may occasionally mispredict a conditional branch instruction as taken and incorrectly mark subsequent states as overfetch. The following step may be taken to correct this:

- Roll the first incorrectly marked state to the top of the listing screen and select the Invasm key.

Disabling the Instruction Cache

The cacheability of areas of 403 memory space is controlled by bits in the Instruction Cache Control Register (ICCR)with a 128 megabyte granularity. For example, to disable the instruction cache for addresses 78000000 through 7FFFFFFF, the following code sequence could be used:

```
mfdcr   r1,ICCR
rlwinm  r1,r1,0,16,14 #   clear bit 15
mtdcr   ICCR,r1       #    disable i cache 78000000..7FFFFFFF
```

3

Preprocessor Interface Hardware Reference

Preprocessor Interface Hardware Reference

This chapter contains reference information on the HP2468A hardware including product, electrical, and environmental characteristics, signal mapping, a brief theory of operation, and repair information.

Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the preprocessor interface.

Table 12. HP E2468A Characteristics

Product Characteristics		
Microcontroller Supported	IBM PowerPC 403GA.	
Package Supported	160-pin PQFP.	
Accessories Required	HP E5335A 160-pin PQFP probe adapter.	
Logic Analyzer Required	HP 16550A, HP 16554A, HP 16555A, HP 16556A, HP 1660, and HP 1661.	
Number of Probes Used	Up to eight 16-channel probes. Five probes are required for inverse assembly.	
Additional Capabilities	The logic analyzer captures all bus cycles.	
Electrical Characteristics		
Power Requirements	None.	
Signal Line Loading	100 Kohms.	
Maximum Clock Speed	33 MHz Clock Input using the HP 1660A/61A, HP 16550A, HP 16554A, HP 16555A, or HP 16556A.	
Target Signal Timing	The HP 1660A/61A, HP 16550A, and HP 16555A Logic Analyzers require a 3.5 ns of combined setup and hold time relative to the analyzer clock.	
Environmental Characteristics		
Temperature	Operating	0 to + 55 degrees C +32 to +131 degrees F
	Nonoperating	-40 to + 75 degrees C -40 to +167 degrees F
Altitude	Operating	4,600 m (15,000 feet)
	Nonoperating	15,3000 m (50,000 feet)
Humidity	Up to 90% noncondensing. Avoid sudden , extreme temperature changes which could cause condensation on the circuit board.	

Signal-to-Connector Mapping

The following tables show the electrical signal-to-connector mapping required by the HP E2468A Preprocessor Interface.

Table 13. PowerPC 403GA Logic Analyzer Interface Signal List - Pod P1

LA bit	403GA pin	signal name	analyzer labels		
clk1	22	SysClk			
15	11	BootW	BootW		STAT
14	12	BusErr	BusErr		STAT
13	136	Error	Error		STAT
12	134	HoldAck	HldAck		STAT
11	122	WBE0 A4	WBE0	WBE0:3	STAT
10	123	WBE1 A5	WBE1	WBE0:3	STAT
9	92	A6			ADDR
8	93	A7			ADDR
7	94	A8			ADDR
6	95	A9			ADDR
5	96	A10			ADDR
4	97	A11			ADDR
3	98	A12			ADDR
2	99	A13			ADDR
1	103	A14			ADDR
0	104	A15			ADDR

Table 13. PowerPC 403GA Logic Analyzer Interface Signal List - Pod P2

LA bit	403GA pin	signal name	analyzer label
clk1	13	Ready	
15	105	A16	ADDR
14	106	A17	ADDR
13	107	A18	ADDR
12	108	A19	ADDR
11	109	A20	ADDR
10	110	A21	ADDR
9	112	A22	ADDR
8	113	A23	ADDR
7	114	A24	ADDR
6	115	A25	ADDR
5	116	A26	ADDR
4	117	A27	ADDR
3	118	A28	ADDR
2	119	A29	ADDR
1		gnd	ADDR
0		gnd	ADDR

Table 13. PowerPC 403GA Logic Analyzer Interface Signal List - Pod P3

LA bit	403GA pin	signal name	analyzer label
clk1	134	HoldAck	
15	42	D0	DATA
14	43	D1	DATA
13	44	D2	DATA
12	45	D3	DATA
11	46	D4	DATA
10	47	D5	DATA
9	48	D6	DATA
8	51	D7	DATA
7	52	D8	DATA
6	53	D9	DATA
5	54	D10	DATA
4	55	D11	DATA
3	56	D12	DATA
2	57	D13	DATA
1	58	D14	DATA
0	62	D15	DATA

Table 13. PowerPC 403GA Logic Analyzer Interface Signal List - Pod P4

LA bit	403GA pin	signal name	analyzer label
clk1	6	TCK	
15	63	D16	DATA
14	64	D17	DATA
13	65	D18	DATA
12	66	D19	DATA
11	67	D20	DATA
10	68	D21	DATA
9	71	D22	DATA
8	72	D23	DATA
7	73	D24	DATA
6	74	D25	DATA
5	75	D26	DATA
4	76	D27	DATA
3	77	D28	DATA
2	78	D29	DATA
1	79	D30	DATA
0	82	D31	DATA

Table 13. PowerPC 403GA Logic Analyzer Interface Signal List - Pod P5

LA bit	403GA pin	signal name	analyzer labels		
clk1	22	SysCLK			
15	31	INT0	Intr 0	Intrpt	STAT
14	32	INT1	Intr 1	Intrpt	STAT
13	33	INT2	Intr 2	Intrpt	STAT
12	34	INT3	Intr 3	Intrpt	STAT
11	35	INT4	Intr 4	Intrpt	STAT
10	36	CINT	Crit In	Intrpt	STAT
9	124	WBE2 A30	WBE2	WBE0:3	STAT
8	125	WBE3 A31	WBE3	WBE0:3	STAT
7	127	R/W-	R/-W	TS0:6	STAT
6	17	ES0 TS0	ES0:2	TS0:6	STAT
5	18	ES1 TS1	ES0:2	TS0:6	STAT
4	19	ES2 TS2	ES0:2	TS0:6	STAT
3	86	BTS TS3	BTS	TS0:6	STAT
2	85	DMA- TS4	-DMA	TS0:6	STAT
1	84	I/D- TS5	I/D-	TS0:6	STAT
0	83	IOTV TS6	IOTV	TS0:6	STAT

Table 13. PowerPC 403GA Logic Analyzer Interface Signal List - Pod P6

LA bit	403GA pin	signal name	analyzer labels	
clk1	13	Ready		
15	14	HoldReq	Hold	
14	134	Reset-	Reset-	
13	135	BusReq	BusReq	
12	139	MuxSel	AmuxS	
11	2	Req0	-DMAR0	Req0:3
10	3	Req1	-DMAR1	Req0:3
9	4	Req2	-DMAR2	Req0:3
8	5	Req3	-DMAR3	Req0:3
7	156	Ack0	-DMAA0	Ack0:3
6	157	Ack1	-DMAA1	Ack0:3
5	158	Ack2	-DMAA2	Ack0:3
4	159	Ack3	-DMAA3	Ack0:3
3	128	EOT0	-EOT0	EOT0:3
2	131	EOT1	-EOT1	EOT0:3
1	132	EOT2	-EOT2	EOT0:3
0	133	EOT3	-EOT3	EOT0:3

Table 13. PowerPC 403GA Logic Analyzer Interface Signal List - Pod P7

LA bit	403GA pin	signal name	analyzer labels		
clk1	134	HoldAck			
15	155	CS0	CS0:7		
14	154	CS1	CS0:7		
13	153	CS2	CS0:7		
12	152	CS3	CS0:7		
11	13	Ready	Ready		
10	126	OE	OE		
9	137	DramOE	DramOE		
8	138	DramWE	DramWE		
7	145	CAS3	CAS3	CAS3:0	
6	144	CAS2	CAS2	CAS3:0	
5	143	CAS1	CAS1	CAS3:0	
4	142	CAS0	CAS0	CAS3:0	
3	151	CS4/RAS3	CS4 RAS3	CAS0:7	RAS3:0
2	148	CS5/RAS2	CS5 RAS3	CAS0:7	RAS3:0
1	147	CS6/RAS1	CS6 RAS3	CAS0:7	RAS3:0
0	146	CS7/RAS0	CS7 RAS3	CAS0:7	RAS3:0

Table 13. PowerPC 403GA Logic Analyzer Interface Signal List - Pod P8

LA bit	403GA pin	signal name	analyzer label
clk1	6	TCK	TCLK
15	7	TMS	TMS
14	8	TDI	TDI
13	16	TDO	TDO
12	9	Halt-	Halt
11	26	SerClk	SerClk
10	27	RecvD	RecvD
9	87	XmitD	XmitD
8	88	DTR/RTS	-DTR -RTS
7	28	DSR/CTS	-DSR -CTS
6	25	Timer	TimClk
5	23	TestA	Test A
4	24	TestB	Test B
3	--	--	
2	--	--	
1	37	FrqR0	FreqR0
0	38	FrqR1	FreqR1

Circuit Board Dimensions

The following figure gives the dimensions for the preprocessor interface assembly. The dimensions are listed in inches and millimeters.

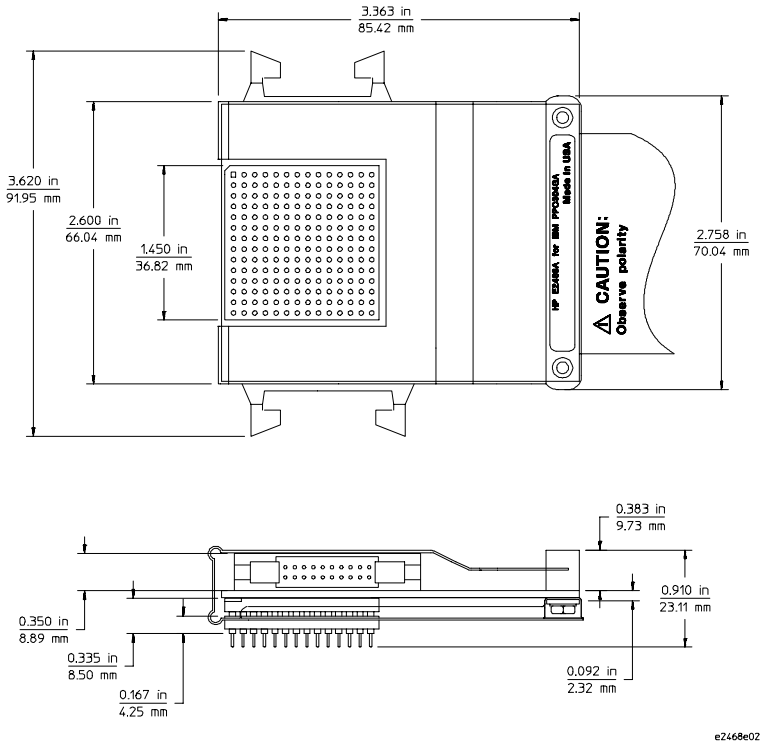

Figure 11. Dimensions

Repair Strategy

The repair strategy for this preprocessor interface is board replacement. However, the following table lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales Office for further information on servicing the board.

Table 13. Replaceable Parts

HP Part Number	Description
E2468-66501	Circuit board assembly
E2468-68700	Inverse assembler disk pouch
E2468-44101	ESD Cover
1200-1874	14x14 PGA pin protector socket

The HP E2468A is a totally passive preprocessor. Boards are tested for shorts and opens and should, therefore, have neither.

If signals are not being correctly passed from the target system to the logic analyzer, check for bent or broken pins on the PGA socket or the pod cable connectors. If damage is visible on the PGA socket, it may be replaced. If a pod cable connector is damaged or if no damage is visible, board replacement is necessary.

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About this edition

This is the first edition of the *HP E2468A PowerPC 403GA Preprocessor Interface User's Guide*. Edition dates are as follows:

1st edition, July, 1995

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